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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/849,191	05/20/2004	Tsukasa Shiraishi	2004-0787	7292

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/849,191	SHIRAISHIET AL	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/725,283.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/849191 Attorney's Docket #: 2004_0787
Filing Date: 5/20/2004; claimed foreign priority to 11/29/2000

Applicant: Shiraishi et al.

Examiner: Alexander Williams

Applicant's election without traverse of species figure 6 (claims 1 to 3), filed 5/12/05, has been acknowledged.

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/725283, filed on 11/29/00. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claim 1 is rejected under 35 U.S.C. § 102(e) as being anticipated by Moresco (U.S. Patent # 6,535,398 B1).

1. Moresco (figures 1 to 9) specifically figure show a semiconductor device module **10** comprising: a semiconductor device including: a multi-layer wiring board which comprises insulation layers **112-116** and circuit pattern layers **121-126,131-134** laminated alternately and is provided with a three-dimensional wiring comprising said circuit pattern layers provided on both sides of the insulation layer and a plurality of inner via holes penetrating through each of said insulation layers and electrically connecting; at least a first semiconductor element **20,30** mounted on the one side of the multi-layer wiring board and a second semiconductor element **4** mounted an the other side of said multi-layer wiring board wherein electrodes of said semiconductor elements are connected with each other by means of said three-dimensional wiring; and a mother multi-layer wiring board having a circuit pattern formed on said surface thereof, wherein said semiconductor device is mounted on said mother multi-layer wiring board and said semiconductor device and said mother multi-layer wiring board are connected by electrical connection means **40**.

Claims 1 to 3 are rejected under 35 U.S.C. § 102(e) as being anticipated by Yew et al. (U.S. Patent # 6,137,164).

1. Yew et al. (figures 1 to 8) specifically figure 8 show a semiconductor device module comprising: a semiconductor device including: a multi-layer wiring board which comprises insulation layers **880** and circuit pattern layers **823** laminated alternately and is provided with a three-dimensional wiring comprising said circuit pattern layers provided on both sides of the insulation layer and a plurality of inner via holes penetrating through each of said insulation layers and electrically connecting; at least a first semiconductor element **803** mounted on the one side of the multi-layer wiring board and a second semiconductor element **804** mounted an the other side of said multi-layer wiring board wherein electrodes of said semiconductor elements are connected with each other by means of said three-dimensional wiring; and a mother multi-layer wiring board **(board connected to 841)** having a circuit pattern formed on said surface thereof, wherein said semiconductor device is mounted on said mother multi-layer wiring board and said semiconductor device and said mother multi-layer wiring board are connected by electrical connection means **841**.

2. The module of the semiconductor device according to claim 1, Yew et al. show wherein said electrical connection means **841** is a projecting electrode which is interposed between said multi-layer wiring board of said semiconductor device and said mother multi-layer wiring board by bonding said back surface of said second semiconductor element onto said mother multi-layer wiring board thus placing said semiconductor device on said mother multi-layer wiring board, thereby to connect said circuit pattern provided on said multi-layer wiring board and said circuit pattern provided on said mother multi-layer wiring board.

3. The module of the semiconductor device according to claim 1, Yew et al. show wherein said electrical connection means is an electrically conductive supporting body which is electrically connected to said wiring in said multi-layer wiring board of said semiconductor device and is also used to fasten said semiconductor device onto said mother multi-layer wiring board, so as to establish electrical connection between said wiring of said multi-layer wiring board of said semiconductor device and said circuit pattern provided on said mother multi-layer wiring board by fastening said semiconductor device onto said mother multi-layer wiring board via said electrically conductive supporting body.

Claims 1 to 3 are rejected under 35 U.S.C. § 102(e) as being anticipated by Isaak et al. (U.S. Patent Application Publication # 2002/0053728 A1).

1. Isaak et al. (figures 1 to 10) specifically figure 10 show a semiconductor device module **470** comprising: a semiconductor device including: a multi-layer wiring board **414** which comprises insulation layers (inherent) and circuit pattern layers (inherent) laminated alternately and is provided with a three-dimensional wiring comprising said circuit pattern layers provided on both sides of the insulation layer and a plurality of inner via holes penetrating through each of said insulation layers and electrically connecting; at least a first semiconductor element **472** mounted on the one side of the multi-layer wiring board and a second semiconductor element **472** mounted an the other side of said multi-layer wiring board wherein electrodes of said semiconductor elements are connected with each other by means of said three-dimensional wiring; and a mother multi-layer wiring board **(bottom portion in which 435 sits)** having a circuit pattern formed on said surface thereof, wherein said semiconductor device is mounted on said mother multi-layer wiring board and said semiconductor device and said mother multi-layer wiring board are connected by electrical connection means **434**.

2. The module of the semiconductor device according to claim 1, Isaak et al. show wherein said electrical connection means **434** is a projecting electrode which is interposed between said multi-layer wiring board of said semiconductor device and said mother multi-layer wiring board by bonding said back surface of said second semiconductor element onto said mother multi-layer wiring board thus placing said semiconductor device on said mother multi-layer wiring board, thereby to connect said circuit pattern provided on said multi-layer wiring board and said circuit pattern provided on said mother multi-layer wiring board.

3. The module of the semiconductor device according to claim 1, Isaak et al. show wherein said electrical connection means **434** is an electrically conductive supporting body which is electrically connected to said wiring in said multi-layer wiring board of said semiconductor device and is also used to fasten said semiconductor device onto said mother multi-layer wiring board, so as to establish electrical connection between said wiring of said multi-layer wiring board of said semiconductor

device and said circuit pattern provided on said mother multi-layer wiring board by fastening said semiconductor device onto said mother multi-layer wiring board via said electrically conductive supporting body.

Claims 1 to 3 are rejected under 35 U.S.C. § 102(e) as being anticipated by Lin et al. (U.S. Patent # 6,768,208 B2).

1. Lee et al. (figures 1 to 6) specifically figure 2A show a semiconductor device module **20A** comprising: a semiconductor device including: a multi-layer wiring board **PCB3** which comprises insulation layers (inherent) and circuit pattern layers **GP,PP** laminated alternately and is provided with a three-dimensional wiring comprising said circuit pattern layers provided on both sides of the insulation layer and a plurality of inner via holes penetrating through each of said insulation layers and electrically connecting; at least a first semiconductor element **CH3** mounted on the one side of the multi-layer wiring board and a second semiconductor element **CH4** mounted an the other side of said multi-layer wiring board wherein electrodes of said semiconductor elements are connected with each other by means of said three-dimensional wiring; and a mother multi-layer wiring board **PCB2** having a circuit pattern formed on said surface thereof, wherein said semiconductor device is mounted on said mother multi-layer wiring board and said semiconductor device and said mother multi-layer wiring board are connected by electrical connection means **BSB**.

2. The module of the semiconductor device according to claim 1, Lee et al. show wherein said electrical connection means **BSB** is a projecting electrode which is interposed between said multi-layer wiring board of said semiconductor device and said mother multi-layer wiring board by bonding said back surface of said second semiconductor element onto said mother multi-layer wiring board thus placing said semiconductor device on said mother multi-layer wiring board, thereby to connect said circuit pattern provided on said multi-layer wiring board and said circuit pattern provided on said mother multi-layer wiring board.

3. The module of the semiconductor device according to claim 1, Lee et al. show wherein said electrical connection means **BSB** is an electrically conductive supporting body which is electrically connected to said wiring in said multi-layer wiring board of

said semiconductor device and is also used to fasten said semiconductor device onto said mother multi-layer wiring board, so as to establish electrical connection between said wiring of said multi-layer wiring board of said semiconductor device and said circuit pattern provided on said mother multi-layer wiring board by fastening said semiconductor device onto said mother multi-layer wiring board via said electrically conductive supporting body.

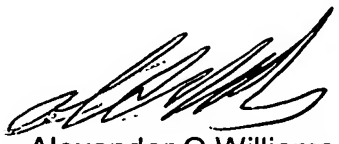
The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686,685,723,777,778,734,668,779,700,701,758,691,698,E25.013,E23.114, 361/767,768,803,818,792,760,763,782,784,794,795	7/21/05
Other Documentation: foreign patents and literature in 257/686,685,723,777,778,734,668,779,700,701,758,691,698,E25.013,E23.114, 361/767,768,803,818,792,760,763,782,784,794,795	7/21/05
Electronic data base(s): U.S. Patents EAST	7/21/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
7/21/05